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EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/863,103	LAMBINO ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Amendment dated 10/15/2004

2. Claims 1-28 are presented for examination.

Claim Objections

3. Claim 9 is objected to because of the following informalities: "a system" on line 2 of the claim should be changed to "the system" because it currently fails to particularly point and distinctly claim which system the recitation is being claimed. Appropriate correction is required.

4. Applicant's arguments with respect to claim 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-8, 12-21 and 24-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Miller, U.S. Patent 5,960,445.

7. Regarding claim 1, Miller teaches a method comprising:

a. receiving a boot block into a secondary location (col. 5, lines 44-50);

b. pointing an execution address to the secondary location, wherein the execution address is the address from which a processor executes instruction when a system is turned on (flag used to boot from backup boot block, col. 5, line 65 through col. 6, line 9 and col. 7, lines 4-42);

c. copying the boot block from the secondary location to a primary location (when counter reaches a fixed value, col. 6, lines 53-58); and

d. pointing the execution address to the primary location (the address to primary location must be pointed to in order to allow PC to boot, col. 7, lines 4-42);

8. Regarding claim 2, Miller taught the method according to claim 1, as described above. Miller further taught pointing an execution address to the secondary location further comprising inverting an address bit of the execution address (col. 6 lines 2-10, col. 7 lines 4-42 and col. 8 lines 20-26). Specifically, Miller discloses using a bit to determine where the execution address is pointed. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1".

9. Regarding claim 3, Miller taught the method according to claim 2, as described above. Miller further taught inverting an address bit of the execution address further comprising inverting address bit sixteen of the execution address (col. 8 lines 20-34).

10. Regarding claim 4, Miller taught the method according to claim 1, as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location (col. 6 line 33 through col. 7 line 7). Specifically,

Miller discloses that the copying of boot block is complete when a comparison between the primary location (first region) and the secondary location (second region) produces a match, which is interpreted to be confirming that copying is complete.

11. Regarding claim 5, Miller taught the method according to claim 1, as described above. Specifically, Miller discloses using a bit to determine where the execution address is pointed [col. 6 lines 2-10 and col. 7 lines 4-7]. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1" and is de-inverted when the bit changes from a "1" to a "0".

12. Regarding claim 6, Miller teaches a system comprising:

a. a processor (inherent within the PC, col. 4, lines 19-23);

b. a flash memory comprising a primary location and a secondary location (EPROM, col. 4, lines 45-48);

c. a boot block executed from the primary location, wherein the boot block further:

i. receives a second boot block in the secondary (boot block code is copied from first to second block region, col. 5, lines 44-50);

ii. points an execution address to the secondary location (flag used to boot from backup boot block, col. 5, line 65 through col. 6, line 9 and col. 7, lines 4-42);

iii. copies the second boot block to the primary location (when counter reaches a fixed value, col. 6, lines 53-58);

iv. points the execution address to the primary location (to allow PC to boot, col. 7, lines 4-7).

13. Regarding claim 7, Miller taught the system according to claim 6, as described above. Miller further teaches an address conversion mechanism for moving the execution address (changing the boot-in-progress flag, col. 7 lines 4-42).

14. Regarding claim 8, Miller taught the system according to claim 6, as described above. Miller further taught a non-volatile storage for storing the second boot block (flash memory is non-volatile memory).

15. Regarding claim 12, Miller teaches a method therefore Miller also teaches the article comprising a medium storing instruction for enabling a processor-based system to:

a. receiving a new boot block into a secondary location (col. 5, lines 44-50);

b. pointing an execution address to the secondary location, wherein the execution address is the address from which a processor executes instruction when a system is turned on (flag used to boot from backup boot block, col. 5, line 65 through col. 6, line 9 and col. 7, lines 4-42);

c. copying the new boot block from the secondary location to a primary location (when counter reaches a fixed value, col. 6, lines 53-58); and

d. pointing the execution address to the primary location (the address to primary location must be pointed to in order to allow PC to boot, col. 7, lines 4-42);

16. Regarding claim 13, Miller taught the method according to claim 12, as described above. Miller further taught pointing an execution address to the secondary location further comprising inverting an address bit of the execution address (col. 6 lines 2-10, col. 7 lines 4-42 and col. 8

lines 20-26). Specifically, Miller discloses using a bit to determine where the execution address is pointed. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1".

17. Regarding claim 14, Miller taught the method according to claim 13, as described above. Miller further taught inverting an address bit of the execution address further comprising inverting address bit sixteen of the execution address (col. 8 lines 20-34).

18. Regarding claim 15, Miller taught the method according to claim 12, as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location (col. 6 line 33 through col. 7 line 7). Specifically, Miller discloses that the copying of boot block is complete when a comparison between the primary location (first region) and the secondary location (second region) produces a match, which is interpreted to be confirming that copying is complete.

19. Regarding claim 16, Miller taught the method according to claim 12, as described above. Specifically, Miller discloses using a bit to determine where the execution address is pointed (col. 6 lines 2-10 and col. 7 lines 4-7). If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1" and is de-inverted when the bit changes from a "1" to a "0".

20. Regarding claim 20, Miller teaches a system comprising:

a. a processor (CPU) [col. 4 lines 45-49];

b. a flash memory comprising a primary location (first writable segment/first region) and a secondary location (second writable segment/second region, col. 3 lines 31-36, col. 5 line 45 through col. 6 line 10 and figure 3); and

c. a boot block executed from the primary location wherein the boot block further:

i. is copied to the secondary location (col. 3 lines 31-36, col. 5 line 45 through col. 6 line 10 and figure 3);

ii. modifies an address bit (a flag such as hardware sticky bit) of an execution address to point to the secondary location (col. 5 line 65 through col. 6 line 2 and col. 7, lines 4-42).

iii. maintains the state of the modified address bit of the execution address following a power cycle (if a reset occurs the flag will still be set, col. 6 lines 4-9); and

iv. copies a new boot block (update first block) to the primary location [figure 3 and col. 5 line 65 et seq.]

v. points the execution address to the primary location (the PC will be allowed to boot from code in the primary location, therefore the execution address must point to the primary location, col. 7 lines 4-7).

21. Regarding claim 21, Miller teaches the system according to claim 20, as described above. Miller further teaches an address conversion mechanism (boot in progress flag) for moving the execution address (flag determines where execution will begin, col. 6 lines 2-10 and col. 7 lines 4-7).

22. Regarding claims 17 and 24, Miller taught the claimed system according to claim 20. Therefore, Miller also teaches the claimed method of using and the claimed article comprising a medium for storing instructions to enable such a system as the limitations of the method and the article appear to be same as that of the system.

23. Regarding claim 18, Miller taught the method according to claim 17 as described above. Miller further taught wherein pointing an execution address to the secondary location further comprising inverting an address bit of the execution address (col. 6 lines 2-10 and col. 7 lines 4-42). Specifically, Miller discloses using a bit to determine where the execution address is pointed. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location.

24. Regarding claim 19, Miller taught the method according to claim 17 as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location (col. 6 line 33 through col. 7 line 7). Specifically, Miller discloses that the copying of boot block is complete when a comparison between the primary location (first region) and the secondary location (second region) produces a match.

25. Regarding claim 25, Miller taught the article according to claim 24 as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location (col. 6 line 33 through col. 7 line 7). Specifically, Miller discloses that the copying of boot block is complete when a comparison between the primary location (first region) and the secondary location (second region) produces a match, which is interpreted to be confirming that copying is complete.

26. Regarding claim 26, Miller teaches a method comprising:

a. receiving an upgrade program into a secondary location (col. 5, lines 44-50);

b. pointing an execution address to the secondary location, wherein the execution address is the address from which a processor executes instruction when a system is turned on (flag used to boot from backup boot block, col. 5, line 65 through col. 6, line 9 and col. 7, lines 4-42);

c. copying the new boot block from the secondary location to a primary location (when counter reaches a fixed value, col. 6, lines 53-58); and

d. pointing the execution address to the primary location (the address to primary location must be pointed to in order to allow PC to boot, col. 7, lines 4-42 and col. 8 lines 20-34);

27. Regarding claims 27 and 28, Miller taught the method according to claim 26 as described above. Miller further teaches modifying a logic component (an address bit) such that an execution address is pointed to the secondary location (Miller modifies a bit which causes the address to point to the secondary location, col. 7 lines 4-42).

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, U.S. Patent 6,308,265 in view of Tamori et al., U.S. Patent 5,960,445.

30. Regarding claim 9, Miller taught the system according to claim 6 as described above. Miller does not disclose a network interface card for connecting a system to a network and for downloading the second boot block to the system.

Tamori teaches a network interface card for connecting a system to a network and for downloading the second boot block to the system (BIOS code, col. 7, lines 3-7). Tamori suggests to those of ordinary skill in the art that updating the boot block by downloading the boot block over a network would have the advantage of easily having access the latest boot block, which would increase usability, functionality and reliability over other methods of obtaining the boot block.

It would have been obvious to one of ordinary skill in the art, having the teachings of Miller and Tamori before them at the time the invention was made to modify Miller to include the network interface card of Tamori to obtain downloading the boot block over a network.

One of ordinary skill would have been motivated to make this modification in order to achieve the advantage of easily having access to the latest boot block, which would increase usability, functionality and reliability over other methods of obtaining the boot block in view of the teachings of Tamori.

31. Claims 10-11 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, U.S. Patent 6,308,265.

32. Regarding claim 10, Miller taught the system according to claim 6 as described above. Miller teaches maintaining the state of an address bit ("sticky bit") following a power cycle (power failure, power up or a reset col. 5 line 65 through col. 6 line 10). Specifically, Miller discloses using a flag that holds the state of an execution address bit. The flag is set in a latch or a flip-flop and is maintained during a power failure, power up or a reset.

Miller does not expressly disclose using a backup battery for maintaining the state of the address bit. Specifically, Miller is silent as to the power source used to maintain the state of the address bit. Miller suggests using a latch or flip-flop. In order for the state of the latches and flip-flops to be maintained power must be supplied to them. Thus, it is necessary in Miller that another power supply must supply power the latch or flip-flop. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a backup battery to supply power to the latch or flip-flop maintaining the state of the address bit. One of ordinary skill in the art would be motivated to use a battery because batteries are small reliable devices and its power is available during even during a power cycle or power failure.

33. Regarding claim 11, Miller taught the system according to claim 6 as described above. Miller further teaches that jumper may be used for adjusting the address bit (col. 7 line 63 through col. 8 line 34). Miller teaches that the jumper may be used if no hardware exists in the PC to physically cause the adjustment of the address bit.

34. Regarding claim 22, claim 22 is rejected for the same reasons used to reject claim 10 above.

35. Regarding claim 23, Miller taught the system according to claim 22 as described above. Miller further teaches that jumper may be used for adjusting the address bit (col. 7 line 63

through col. 8 line 34). Miller teaches that the jumper may be used if no hardware exists in the PC to physically cause the adjustment of the address bit.

Conclusion

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
December 30, 2004

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